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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,929	05/24/2001	Min-hwa Chi	004192.P053D	4893

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EXAMINER

KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	3

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

9/11

Office Action Summary	Application No.	Applicant(s)
	09/865,929	CHI, MIN-HWA
	Examiner	Art Unit
	Donghee Kang	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 24 May 2001.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 11-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 15-18 is/are rejected.
- 7) Claim(s) 11-14 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. This application appears to be a division of Application No. 09/286,946, filed April 8, 1999. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth only that portion of the earlier disclosure which is germane to the invention as claimed in the divisional application.

Specification

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Antecedent basis for the claimed subject matter in claim 15, in lines 7, 10, 14, & 22-23 are required, namely:

the "a first gate structure formed atop said n-well", "a second gate structure formed atop said n-well", "a n+ structure being the output of said NAND logic circuit", and "said second switch also electrically connected to said n+ structure" which are not disclosed in the description section of the specification.

Claim Objections

4. Claims **11** and **15** are objected to because of the following informalities:

Regarding claims **11 & 15**, line 10, respectively: the phrase “said first gate structure being the second input” is misdescriptive. The “said first gate structure” should be the “said second gate structure”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **15-18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim **15**, line 7: the phrase “a first gate structure formed atop said n-well” is misdescriptive. This interpretation seems to be inconsistent with Fig.10a, because fig.10a does not show the first gate structure formed atop said n-well.

Regarding claim **15**, line 10: the phrase “a second gate structure formed atop said n-well” is misdescriptive because fig.10a does not show the second gate structure formed atop said n-well.

Regarding claim **15**, line 14: the phrase “a n+ structure being the output of said NAND logic circuit” is misdescriptive. In the figure 10a, a p+ structure is the output of the NAND logic circuit.

Regarding claim 15, lines 22-23: the phrase "said second switch also electrically connected to said n+ structure" is misdescriptive. Fig.10a does not show the above limitation and the written description does not disclose the above limitation.

Claims 16-18 are rejected since each includes the limitations of independent claim 15.

Allowable Subject Matter

7. Claims 11-14 are objected due to informalities, but would be allowable if rewritten to overcome the informalities.
8. Claims 15-18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.
9. The following is a statement of reasons for the indication of allowable subject matter:

No prior art teaches a NAND logic circuit comprising:

a thin transistor formed on thin SOI where the thin transistor has gated n+ and p+ junctions, which serve as switches turning on and off GIDL current on the surface of the junction; a first gate structure formed atop a p-well, said first gate structure being the first input and connected to a first switch; a second gate structure formed atop a p-well, said second gate structure being the second input and connected to a second switch; a p+ structure formed adjacent to a first edge of said first and second gate structures, said p+ structure being the output of said NAND logic circuit; and a n+ structure adjacent a second edge of said first and second gate structures.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DHK
September 26, 2002

Stan Lohr